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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,849	03/30/2004	Seong Cheol Kang	LT-0051	2338

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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,849	KANG, SEONG CHEOL	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh(US PGPub 2003/0056123).

As to claim 1, Hsieh discloses a method for controlling CPU speed(frequency of CPU; see paragraph 0032, lines 7-8) transition, comprising receiving a System Management Interrupt (SMI) signal(output; see paragraph 0032, line 6)(see paragraph 0032, lines 6-13), determining whether a bus master device(peripherals; see paragraph 0032, line 9) is in an active state when the SMI signal is for performing CPU speed transition(see paragraph 0032, lines 16-20), and canceling the CPU speed transition operation when the bus master device is in the active state(see paragraph 0035, lines 26-28) and generating at prescribed intervals a retry SMI signal(see paragraph 0034).

As to claim 2, Hsieh discloses the method of comprising performing the CPU speed transition operation when the bus master device is not in the active state(see paragraph 0033, lines 1-3).

As to claim 3, Hsieh discloses the method wherein the retry SMI signal generated at prescribed intervals is one of a watchdog timer SMI signal and an embedded control SMI signal to retry the CPU speed transition operation(see paragraph 0032, lines 4-13).

As to claim 4, Hsieh discloses the method wherein the determining comprises disabling occurrences of additional watchdog timer SMI signals when the received SMI signal is the watchdog timer SMI signal to retry the CPU transition operation, and re-determining whether the bus master device is in the active state(see paragraph 0032, lines 4-13).

As to claim 5, Hsieh discloses the method wherein the determining comprises disabling occurrence of additional embedded controller SMI signals when the received SMI signal is an embedded controller SMI signal to retry the CPU speed transition operation, and re-determining whether the bus master device is in the active state(see paragraph 0032, lines 4-13).

As to claim 6, Hsieh discloses the method wherein the determining comprises performing a prescribed operation corresponding to the received SMI signal when the received SMI signal is not an SMI signal for CPU speed transition, the watchdog timer SMI signal to retry the CPU speed transition operation or the embedded controller SMI to retry the CPU speed transition operation(see paragraph 0032, lines 4-13).

As to claim 7, Hsieh discloses the method wherein the SMI signals are at least one of a hardware generated signal and an application program generated signal(see paragraph 0032, lines 4-13).

As to claim 8, Hsieh discloses a portable computer(hand-held information processing apparatus; see paragraph 0032, lines 2-3), comprising a CPU(CPU; see paragraph 0032, line 8) configured to operate using at least two speeds, a controller(frequency-adjusting module in CPU 202, see Fig. 6) configured to perform a prescribed operation to transition between the at least two speeds of the CPU(frequency of CPU; see paragraph 0032, lines 7-8), and an interrupt occurrence reason recognition means for recognizing an occurrence reason of an interrupt signal(output; see paragraph 0032, line 6)(see paragraph 0032, lines 6-13). Hsieh also discloses an active state checking means(peripheral busy setting register 204, see Fig. 6) for checking an active state of a predetermined device(peripherals; see paragraph 0032, line 9)(see paragraph 0032, lines 16-20), and interrupt generating means for creating a second interrupt signal to retry the prescribed operation(see paragraph 0034) for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is created for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state(see paragraph 0035, lines 26-28).

As to claim 9, Hsieh discloses the portable computer wherein the interrupt signal for the CPU speed transition is responsive to a change of CPU use amount, switching between AC adapter and battery power sources, reduction of battery lifetime, runtime setup of a user and temperature variation(see paragraph 0032, lines 4-13).

As to claim 10, Hsieh discloses the portable computer wherein the interrupt generating means creates the second interrupt signal using a predetermined timer contained in the system(see paragraph 0034).

As to claim 11, Hsieh discloses the portable computer wherein the predetermined timer contained in the system is a watchdog timer or an inner timer of an embedded controller(see paragraph 0032, lines 4-13).

As to claim 12, Hsieh discloses the portable computer wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS(see paragraph 0032, lines 4-6).

As to claim 13, Hsieh discloses the portable computer wherein the predetermined device is a bus master device(peripherals; see paragraph 0032, line 9).

As to claim 14, Hsieh discloses the portable computer wherein the second interrupt is repeatedly generated until the CPU transition is performed(see paragraph 0032, lines 4-13), and wherein the portable computer is a notebook computer(hand-held information processing apparatus; see paragraph 0032, lines 2-3).

As to claim 15, Hsieh discloses an apparatus, comprising an interrupt receiver configured to receive interrupt signals(see paragraph 0032, lines 6-13), and an interrupt generator coupled to the interrupt receiver and configured to generate a second interrupt signal to retry a prescribed operation(see paragraph 0034) needed for CPU speed(frequency of CPU; see paragraph 0032, lines 7-8) transition when a first interrupt signal(output; see paragraph 0032, line 6) for the CPU speed transition is received and

a bus master device(peripherals; see paragraph 0032, line 9) is in an active state(see paragraph 0032, lines 16-20).

As to claim 16, Hsieh discloses the apparatus wherein the interrupt generator creates the second interrupt signal using a predetermined timer contained in the system(see paragraph 0034).

As to claim 17, Hsieh discloses the apparatus wherein the predetermined timer contained in the system is at least one of a watchdog timer and an inner timer of an embedded controller(see paragraph 0032, lines 4-13).

As to claim 18, Hsieh discloses the apparatus wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS(see paragraph 0032, lines 4-6).

As to claim 19, Hsieh discloses the apparatus wherein the apparatus is in a notebook computer(hand-held information processing apparatus; see paragraph 0032, lines 2-3).

As to claim 20, Hsieh discloses the apparatus wherein the interrupt signals are one of hardware interrupts and software interrupts(see paragraph 0032, lines 4-13).

As to claim 21, Hsieh discloses an article including a machine-readable storage medium containing instructions for controlling CPU speed(frequency of CPU; see paragraph 0032, lines 7-8) transition in a computer system(hand-held information processing apparatus; see paragraph 0032, lines 2-3), said instructions, when executed in the computer system, causing the computer system to receive an System Management Interrupt (SMI) signal(output; see paragraph 0032, line 6)(see paragraph

0032, lines 6-13), determine whether a bus master device(peripherals; see paragraph 0032, line 9) is in an active state when the SMI signal is a first SMI CPU speed transition signal(see paragraph 0032, lines 16-20), and cancel the CPU speed transition operation when the bus master device is in the active state(see paragraph 0035, lines 26-28) and generate at predetermined intervals an event(see paragraph 0034).

As to claim 22, Hsieh discloses the article wherein the event is a second SMI CPU speed transition signal(see paragraph 0032, lines 4-13).

As to claim 23, Hsieh discloses the article wherein the event is one of a hardware interrupt and a software interrupt(see paragraph 0032, lines 4-13).

Response to Arguments

2. Applicant's arguments, see Remarks, filed 12/20/2006, with respect to the rejection(s) of claim(s) 1-23 under Atkinson(US Patent 6,802,015) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hsieh(US PGPub 2003/0056123).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Brown
Art Unit 2116

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/1/07